Oled SSD1306

* **Upplösning:** 128x64 dot matrix panel
* **Spänning:** 1.65V till 3.3V IC logic. 7V till 15V för panel driving

Oscillator finns inbyggt. (CLS-pin) Om CLS-pin = HIGH så är den interna oscillatorn vald.  
Ändra frekvensen med kommandot D5h A [7:4].

**SDAout** = D2-pin,  **SDAin** = D1-pin, **SCL** = D0-pin.

SDA och SCL måste va kopplade med varsin pullupresistor.

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I 2 C-bus. The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format, b7 b6 b5 b4 b3 b2 b1 b0 **0 1 1 1 1 0** SA0 R/W#

“SDAIN” and “SDAOUT” are tied together and serve as SDA. The “SDAIN” pin must be connected to act as SDA. The “SDAOUT” pin may be disconnected. When “SDAOUT” pin is disconnected, the acknowledgement signal will be ignored in the I2 C-bus.

**Write mode for I2C**

**1)** The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 8-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.   
**2)** The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).

**3)** The write mode is established by setting the R/W# bit to logic “0”.   
**4)** An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 8-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.   
**5)** After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.   
 **a.** If the Co bit is set as logic “0”, the transmission of the following information will

contain data bytes only.  
 **b.** The D/C# bit determines the next data byte is acted as a command or a data. If the

D/C# bit is set to logic “0”, it defines the following data byte as a command. If the

D/C# bit is set to logic “1”, it defines the following data byte as a data which will be

stored at the GDDRAM. The GDDRAM column address pointer will be increased by

one automatically after each data write.  
**6)** Acknowledge bit will be generated after receiving each control byte or data byte.   
**7)** The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 8-8. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in Figure 8-13.

Sida 25 finns en bild över displayens struktur.

# Display av och på

**1.** Power ON VDD   
**2.** After VDD become stable, set RES# pin LOW (logic low) for at least 3us (t1) (4) and then HIGH (logic high).

**3.** After set RES# pin LOW (logic low), wait for at least 3us (t2). Then Power ON VCC. (1)

**4.** After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (tAF).

# Kommandon

HEX: 81 A[7:0] För contrast kontroll.  
HEX: AE För att sätt igång displayen.  
HEX: AF För att stänga av displayen.  
HEX: 40~7F Start position ersätt 40 med ett tal mellan 0-63.  
HEX D3 A[5:0] Display offset  
  
  
